REMARKS

The drawings were objected to for including references which are not mentioned in the specification. Applicant has amended the specification as shown above to add the appropriate reference numbers. No new matter has been added. Additionally, applicant proposes one drawing correction to address the "Control Input" concern. Withdrawal of the drawing objection is requested.

The drawings were further objected for failure to illustrate each claimed feature of the invention. In response to this objection, applicant has made amendments to the claims to: delete reference to a tester probe in claims 8 and 29 (claim 6 has been canceled); delete reference to an integrated circuit chip in claims 1-15 (claims 16-21 have been canceled); and delete reference to a counter in claim 45. Additionally, applicants traverse with respect to the second pair of series connected transistors in claim 12 and 33. These transistors are shown as the calibration circuit transistors in Figs. 5 and 7. Applicants also traverse with respect to the control terminal/plate (note: not "plate line") coupling recited in claim 37. Figure 5 in combination with Figs 1A or 1B clearly shows the control terminal of transistor 22 being coupled through the bit line and access transistor T to one plate of the ferroelectric capacitor. Applicant also traverses with respect to the sense amplifier/plate coupling recited in claim 46. Figure 5 in combination with Figs 1A or 1B clearly shows the sense amplifier 10 being coupled through the bit line and access transistor T to one plate of the ferroelectric capacitor.

The claims were rejected as not enabled. The Examiner identified two issues. With respect to issue (A), applicant respectfully submits that the proposed amendments to the specification address the Section 122 issue. With respect to issue (B), applicant respectfully submits that the claim amendments and remarks presented above address the Section 112 issue. Withdrawal of the rejection is requested.

The Examiner rejected a number of claims as being indefinite. With respect to claims 8 and 9, applicants has amended these claims to address the antecedent issue (and a part of claim 8 has been deleted and added to independent claim 1). With respect to claim 11, applicant has amended the claim to address the antecedent issue. With respect to claims 12, 15, 36 and 47, applicant has amended these claims to rename the recited pads (and claim 12 has been converted into independent format). With respect to claim 13, 20 and 34, applicant has amended claims 13 and 34 to emphasize a matching relationship (and claim 13 has been converted to independent format). This calibration operation and the effect of the matching/mapping relationship between current and voltage in the calibration circuit as compared to the bit line is explained in detail in the specification pages 15-16. With respect to claims 14, 35 and 49, applicant has amended claims 14 and 35 to address the antecedent issue. Claim 49 does not appear to have the antecedent issue identified by the Examiner, and thus the rejection is traversed. With respect to claim 33, applicant has amended the claim to rename the pads. With respect to claim 37, applicant has amended the claim to correct the recited connection of the two transistors, pad and reference voltage to match that shown in Figure 5.

Claims 1-37 and 40-49 were rejected under 35 U.S.C 102(b) as being anticipated by the McClure ('007) reference. Claims 6-7, 16-21 and 37-38 have been canceled. Thus, claims 1-5, 8-15, 22-36 and 38-49 are now pending.

Claim 1 has been amended to delete reference to sense amp disable and include some of the limitations of claim 8. The McClure reference fails to teach the plurality of transistor pairs limitation as comprising the test circuit where the control terminal of one transistor in the pair is coupled to the bit line. The McClure reference teaches transistor 24 having its drain terminal coupled to the bit line.

Claim 12 has been amended to include the limitations of original claim 1 (without sense amp disable). The McClure reference fails to teach the first and second pairs of transistors

limitations. Additionally, the McClure reference fails to teach having the control terminal of a first transistor in the first pair be coupled to the bit line (see, above discussion of claim 1).

Claim 13 has been amended to include the limitations of original claim 1 (without sense amp disable). The McClure reference fails to teach the calibration test circuit to provide a matching relationship between current and voltage.

Claims 22 has been amended to delete reference to the sense amp and include some of the limitations of claim 27. The McClure reference fails to teach the pair of transistors and further fails to teach having the control terminal of one transistor in the pair be coupled to the bit line (see, above discussion of claim 1).

Claim 37 distinguishes over McClure because McClure fails to teach the claimed first and second transistors being connected to the ferroelectric capacitor in the manner claimed and further having a first transistor in the pair coupled to the ferroelectric capacitor plate.

In view of the above, withdrawal of the Section 102 rejection is believed to be appropriate. Applicant further submits that the McClure reference is commonly owned with the present application and therefore cannot be used in a Section 103 rejection. Accordingly, this application appears to be in condition for allowance, and such a Notice is respectfully requested.

Applicant notes the obviousness-type double patenting rejection. In view of the amended claims, Applicant respectfully traverses. The test circuit of the present invention (with the pair of series connected transistors, or the pairs of series transistors, or the calibration circuit, and/or combinations of the same) is clearly a patentably distinct invention from the test circuit disclosed and claimed in the McClure reference.

Favorable consideration of the application as now presented is respectfully requested.

Respectfully submitted,

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Date: 11/20/03

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